UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/629,966	07/31/2000	Moshe Gefen	246/68	4504

7590 12/22/2004

Dr. Mark Friedman Ltd
C/O BILL POLKINGHORN - DISCOVER DISPATCH
9003 FLORIN WAY
UPPER MARLBORO, MD 20772

EXAMINER	
ANDERSON, MATTHEW D	
ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 12/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
P.O. BOX 1450
ALEXANDRIA, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/629,966
Filing Date: July 31, 2000
Appellant(s): GEFEN ET AL.

MAILED
DEC 22 2004
Technology Center 2100

Mark M. Friedman
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 11/26/04.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

The following is a listing of the evidence (e.g., patents, publications, Official Notice, and admitted prior art) relied upon in the rejection of claims under appeal.

6,189,070	See et al.	2-2001
4,491,790	Keeley et al.	2-1996

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 29-30 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. There does not appear to be clear support in the original disclosure for the suspending/resuming being effected ***only*** by the memory device. While there is no *in haec verba* requirement, newly added claim limitations must be supported in the specification through express, implicit, or inherent disclosure. The trouble is that there is no such disclosure, easy though it is to imagine it. Purdue Pharma L.P. v. Faulding Inc., 230 F.3d 1320, 1328, 56 USPQ2d 1481, 1487 (Fed. Cir. 2000). The Examiner does not question whether the claim language is inconsistent with, or contradictory to, the teachings of the specification and figure 4. But, the Examiner maintains that the specification does not **clearly and concisely** disclose to the skilled artisan that the inventors considered *this particular* control of processing. There is support for the memory device controlling the suspend/resume processes, but there is no explicit support for nothing else controlling processing. The mere lack of mentioning other elements controlling processing is not sufficient support for claiming that no other elements do so. The written description requirement was not satisfied because the ***disclosure revealed a broad invention from which the later-filed claims carved out a patentable portion***.

Claims 1, 3-4 and 6, 10, 13-14, and 16-30 are rejected under 35 U.S.C. 102(e) as being anticipated by See *et al.* (US Patent # 6,189,070).

With respect to claims 1, 3, and 13-14, See *et al.* disclose:

a host for accessing a non-volatile memory device, as shown by processor 100 of figure 1;

a non-volatile flash array for holding code and data, as disclosed in the abstract and column 1, lines 37-39;

non-volatile circuitry for controlling content and activity of the non-volatile array, as shown by the erase, program, and read circuitry (items 190, 194, and 196 of figure 7);

logic circuit hardware, separate from the host, for enabling automatic suspending and/or automatic resuming of operations in response to a read request, as shown by the suspend circuitry (hardware), items 192 and 195, which is part of the flash device of figure 7, which is separate from the processor in figure 1, while column 3, lines 55-58, which recites a method and apparatus for suspending a non-read operation in a nonvolatile writeable memory in order to read code from the nonvolatile writeable memory.

With respect to claim 4, See *et al.* disclose the logic circuit enabling code execution and data storage/processing facilities within a single chip device with a single silicon die, as disclosed in the abstract and figure 5.

With respect to claim 6, See *et al.* disclose the logic circuit being embedded into a memory chip, as shown in figure 5.

With respect to claims 10 and 13, See *et al.* disclose the logic circuit monitoring the status of the current operations in the memory chip, as shown by the read status circuitry (item 198 in figure 7).

With respect to claim 13, See *et al.* disclose:

adding at least one logic circuit to the non-volatile memory device, as shown by the control circuitry in figures 6 and 7;

monitoring status of current operations in said memory chip by said at least one logic circuit; as shown by the read status circuitry (item 198 in figure 7);

signaling if the device is available for code execution, by said at least one logic circuit, as shown by the suspend and resume latches in figure 7;

commanding the device to suspend and/or resume chip operations, in response to a read request by said at least one logic circuit, by teaching in column 3, lines 55-58, which recites a method and apparatus for suspending a non-read operation in a nonvolatile writeable memory in order to read code from the nonvolatile writeable memory.

With respect to claim 14, See *et al.* disclose

adding at least one logic circuit to work with the a non-volatile memory device, as shown by the control circuitry in figures 6 and 7;

sensing read requests while the device is in program/erase mode/operation by the at least one logic circuit, and in response to the sensing, entering of program and/or erase operations into suspend mode, by teaching in column 3, lines 55-58, which recites a method and apparatus for suspending a non-read operation in a nonvolatile writeable memory in order to read code from the nonvolatile writeable memory;

signaling to CPU/BUS to delay executing said read request, by said at least one logic circuit, turning off signal to allow CPU/BUS to execute said read request, by the at least one logic device, exiting of said device from said suspended mode to continue program/erase operation, by said at least one logic circuit, by teaching in figure 4A-B and in column 3, lines 15-25, enabling and disabling interrupts to allow read and non-read operations, and a check for occurrences of interrupts.

With respect to claim 16, See *et al.* disclose suspend/resume logic circuitry for enabling hardware initiated suspending/resuming of data processing operations, as shown by the suspend circuitry (item 192 and 195 in figure 7).

With respect to claim 17, See *et al.* disclose a non-volatile memory (150), circuitry for read, programming, and erasing said non-volatile memory (140), and a hardware mechanism for suspending an activity of said circuitry in response to at least one read request (column 3, lines 55-58).

With respect to claims 16-17, See *et al.* disclose suspending data processing operations in response to at least one read request received by the memory device, by teaching in column 3, lines 54-58, describe a method and apparatus for suspending a non-read operation in a nonvolatile writeable memory in order to read code from the nonvolatile writeable memory.

With respect to claim 18, See *et al.* disclose the hardware mechanism also is operative to resume said activity of the circuitry after said circuitry has finished processing said at least one read request, as shown by the resume latches in figure 7.

With respect to claim 19, See *et al.* disclose the activity being erasing the non-volatile memory, as shown by the erase latches in figure 7.

With respect to claim 20, See *et al.* disclose the activity being programming the non-volatile memory, as shown by the program latches in figure 7.

With respect to claim 21, See *et al.* disclose the hardware mechanism includes at least one logic circuit, as shown in figure 7.

With respect to claim 22, See *et al.* disclose:

indicating to a host that issued said at least one read request that execution of the read request should be delayed, by teaching in column 3, lines 55-58, which recites a method and apparatus for suspending a non-read operation in a nonvolatile writeable memory in order to read code from the nonvolatile writeable memory;

and subsequently indicating to the host that the memory device is available for reading, as indicated by the read status latch and circuitry in figure 7.

With respect to claim 23, See *et al.* disclose monitoring the processing of the read request to determine when the circuitry has finished processing the read request, by teaching in column 7, lines 39-42, that the status may be provided automatically during read operations while the flash device remains in status mode.

With respect to claim 24, See *et al.* disclose commencing an operation selected by the group consisting of erasing the programming the non-volatile memory device, by the memory device, during said operation, requesting a read operation, by the host, and in response to the request, suspending said operation by the memory device, by teaching in column 3, lines 55-58, which recites a method and apparatus for suspending a non-read (erase/program) operation in a nonvolatile writeable memory in order to read code from the nonvolatile writeable memory.

With respect to claims 25 and 26, See *et al.* disclose that in response to said request, signaling to the host to delay execution of the request, by the memory device, in response to the signal, delaying execution of the request by the host, by teaching in figure 4A-B and in column 3, lines 15-25, enabling and disabling interrupts to allow read and non-read operations, and a check for occurrences of interrupts

With respect to claim 27, See *et al.* disclose signaling the host to resume execution of the request by the memory device, as indicated by the read status latch and circuitry in figure 7, and the Ready/Busy (RY/BY#) pin 62 of the flash device

With respect to claim 28, See *et al.* disclose subsequent to the suspending, monitoring a conclusion of the read request from the host, by the memory device, and upon detecting said conclusion, resuming said operation by the memory device, by teaching in column 8, lines 55-60, that the memory array control circuitry 140 includes a means for storing the state of the suspended non-read operation so that the non-read operation can be resumed later.

With respect to claims 29-30, See *et al.* disclose the suspending/resuming being effected only by the memory device, as shown by the erase/program suspend circuitry (items 192 & 195 in figure 7) and erase and program suspend and resume latches (178 b, c, e, f). These elements are contained within the memory array control circuitry and command register, which are shown in figure 5 to be part in the flash EPROM.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over See *et al.* and Keeley *et al.* (US Patent # 4,491,790).

See *et al.* teach all other limitations of the parent claim, but fail to specifically disclose code execution and data storage/processing within a bank of single memory chips with single silicon dies. Keeley *et al.* teach in column 12, lines 5-8, of an EEPROM array with two banks which is used in a system which can suspend or resume processor operations.

It would have been obvious to one of ordinary skill in the art, having the teachings of See *et al.* and Keeley *et al.* before him at the time the invention was made, to modify the EPROM array in the system which can suspend or resume processor operations taught by See *et al.*, to be a banked EEPROM array, as with the system which can suspend or resume processor operations taught by Keeley *et al.*, to allow parallel access to the banks of the memory device, as taught by Keeley *et al.*.

(11) Response to Argument

With respect to the USC 112 rejections, the Applicant alleges that there is indeed support for the suspending and resuming being effected only by the memory device. In page 9 of the Brief, the Applicant cites Figure 4 and pages 8-9 of the specification to repeatedly argue that suspending and resuming "is managed exclusively by automatic suspend/resume logic". The problem arises though that the specification never does recite the term "exclusively" as alleged by the applicant. As discussed in the previous Office Action, this is the reason for the USC 112 rejection.

While there is no *in haec verba* requirement, newly added claim limitations must be supported in the specification through express, implicit, or inherent disclosure. The trouble is that there is no such disclosure, easy though it is to imagine it. Purdue Pharma L.P. v. Faulding Inc., 230 F.3d 1320, 1328, 56 USPQ2d 1481, 1487 (Fed. Cir. 2000). The Examiner does not

question whether the claim language is inconsistent with, or contradictory to, the teachings of the specification and figure 4. But, the Examiner maintains that the specification does not **clearly and concisely** disclose to the skilled artisan that the inventors considered *this particular* control of processing. There is support for the memory device controlling the suspend/resume processes, but there is no explicit support for nothing else controlling processing. The mere lack of mentioning other elements controlling processing is not sufficient support for claiming that no other elements do so. The written description requirement was not satisfied because the ***disclosure revealed a broad invention from which the later-filed claims carved out a patentable portion***.

This raises the question of what is considered the claimed "memory device". Is it all elements shown within the larger box in figure 4 (flash array and suspend, resume, and bus logic), or merely the flash array 24? Or is it even something outside of the box shown in figure 4 that effects the suspending? To make a similar argument to that made by the Applicant towards the See reference, is it not the CPU making a request over CPU bus 20 and bus logic 21 that initiates the suspend and resume logic? This would seem to be supported by the claimed parts (b) and (c) in claim 24, reading "during said operation, requesting a read operation, ***by the host***; and ***in response to said request***, suspending said operation, by the memory device." Much like the Applicants' own arguments beginning at the bottom of page 14 of the Brief, even though the only hardware recited explicitly in the specification for suspending and resuming is inside the memory device of figure 4, it is clear that the CPU (or host) participates actively in the automatic suspending and resuming operations. Therefore, for the reasons given above, there does not

appear to be explicit support for the claimed limitations of suspending/resuming being effected ***only*** by the memory device.

The Applicant then traverses the USC 102 rejection of claims 1, 3, 4, 6, 10, 13, 14, and 16-30 as being anticipated by See et al. The Applicant argues in page 11 of the Brief that "the difference between the present invention and the invention of See et al. lies in which component is responsible for initiating the suspensions of programming/erasing operations." The Applicant argues that the processor 400 of See initiates suspending and resumption of programming and erasing as needed, and that this is different from the present invention, "in which hardware in the memory device itself initiates the suspension and resumption of the programming/erasing operations in response to read requests from the host system." It is important to note though, that the hardware is only specifically recited in independent claims 16 and 17. And in both these cases, the hardware initiated suspension is claimed to be responsive to a read request from a host (processor). It is also important to note that nothing in the claims explicitly prohibit a processor from being involved in the suspension process. In fact, as mentioned above, the claims state that the suspension is in response to a host (processor) request. Regardless, all that the claims recite is hardware circuitry for performing suspension and resumption. (And technically, only one of either suspend or resume operations due to the "and/or" language in claim 1.) Figure 7 of See clearly shows hardware circuitry which decodes a command to automatically enable the suspend and resume latches and circuitry shown. And even assuming arguendo that the processor of See initiates suspend/resume operations, a processor is also hardware, not software, as it has tangible circuitry. Additionally, as for all independent claims other than 16 and 17 (those not containing

the term "hardware"), the Applicants' arguments requiring hardware initiation are unsubstantiated because such a feature is not claimed.

The Applicant argues repeatedly that See differs from the claimed invention because the processor of See is the one the initiates the suspending/resuming. The Applicant even states in page 14 of the Brief that the suspend/resume circuitry of See "is controlled by commands from processor 400." This seems virtually synonymous to the Applicants' own arguments in page 11 of the Brief, where he adds emphasis to a particular limitation of his own claim by underlining "in response to read requests from the host system." Lines 7-9 of claim 1 clearly state "enabling suspending and/or resuming of operations *in response to a read request from said host*." In other words, the suspending/resuming is initiated by a read request from a host (or processor). **This is exactly how the Applicant argues See performs.** If the Applicant continues to argue against the reference that suspend and resume hardware circuitry within flash EPROM 10 of See is only initiated in response to a request from the processor 400, then the Examiner asks how the claimed logic circuitry for suspending/resuming in response to a request from a host is not also initiated by the host?

The Applicants' memory device shown within the box in his figure 4 appears remarkably similar to that shown by figures 5 and 7 of See. Both contain a memory array accessed through control/logic circuitry containing suspend/resume functionality. By the same token as Applicants' arguments concerning the USC 112, written description rejections, if the present invention's suspend/resume circuitry is initiated *exclusively* by the logic circuits 26 and 27, and not by a host request over CPU bus 20, then how could one alternatively consider the

suspend/resume circuitry contained within the flash EPROM controller of See figure 5 to be initiated by an external processor? Simply put, one cannot.

In summary, the Applicants repeatedly argue that it is solely the hardware circuitry that initiates suspend and resume operations in the present invention. The problem is that only claims 16 and 17 specifically mention hardware, and only claim 16 mentions hardware initiation. If initiation is the question, then all other claims without such an initiation limitation could be broadly interpreted to be initiated by any of a number of different elements. For the sake of argument, this could include a processor separate from the logic circuitry (even though a processor is also considered hardware, and could nonetheless read upon the claimed hardware initiation).

Even with regards to claim 16, though, it is recited that the hardware initiates suspending in response to a host request. As discussed above, See teaches suspend and resume latches and circuitry which automatically performs the actual suspend and resume operations. It is this circuitry that actually executes the suspend and resume functions, not the processor. Once again, similar to the Applicants' arguments in page 10 of the Brief, all the relevant operations are performed only by the suspend and resume circuitry. And as such, See reads upon the limitations of claim 16.

On page 15 of the Brief, the Applicant then argues that the Examiner never addressed the limitation of suspending/resuming in response to a *read* command. As recited in paragraph 6 of the Office Action dated 6/7/04, column 3, lines 55-58, teach a method and apparatus for suspending a non-read (program or erase) operation in a nonvolatile writeable memory in order

to *read* code from the nonvolatile writeable memory. Column 2, lines 45-55, discusses how a processor can use an interrupt to read data from the volatile memory, and column 4, line 44 through column 5, line 10, discusses how this interrupt (i.e., read request) will cause a suspension of a program or erase operation in order to allow the read to occur.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Matthew D. Anderson
Primary Examiner
Art Unit 2186
December 7, 2004

Conferees:

Matthew M. Kim
Supervisory Patent Examiner

Donald Sparks
Supervisory Patent Examiner

DONALD SPARKS
SUPERVISORY PATENT EXAMINER

DR. MARK FRIEDMAN LTD
C/O ANTHONY CASTORINA
2001 JEFFERSON DAVIS HIGHWAY
SUITE 207
ARLINGTON, VA 22202